WHAT IS CLAIMED IS:

1. A method for spectrally shaping nonlinear intersymbol interference (NLISI) in an oversampling digital-to-analog converter causing energy associated with NLISI to fall outside a signal band, the method comprising the steps of:

receiving a multiple bit digital input signal in said signal band;

providing a quantized representation of said multiple bit digital input signal;

providing a first-order shaper circuit for shaping quantization noise;

providing at least one higher-order shaper circuit so as to spectrally shape NLISI; and

changing said quantized representation based on said first order shaper circuit and said at least one higher-order shaper circuit, thereby reducing NLISI energy level present in said signal band.

2. The method of claim 1, wherein the step of providing at least one higher-order shaper circuit comprises the steps of:

calculating said NLISI based on a Volterra model, said Volterra model having at least one term to generate a calculated signal;

filtering said calculated signal to generate a filtered signal; and

providing a bias signal based on said filtered signal.

3. The method of claim 2, wherein the step of calculating said NLISI comprises the steps of:

delaying said quantized representation, thus providing a delayed signal;

multiplying said quantized representation and said delayed signal, thus providing a product signal;

and wherein the step of providing a bias signal comprises the step of

multiplying said filtered signal by said quantized representation.

4. The method of claim 1, wherein said quantized representation is a single-bit representation.

5. An oversampling multi-bit digital to analog converter for converting a multi-bit converter digital input to an analog converter output, comprising:

a digital signal processor that spectrally shapes quantization noise using delta-sigma modulation, the digital signal processor comprising a first order shaper circuit for shaping quantization noise;

a unitary digital-to-analog converter connected to the digital signal processor; and

an analog filter connected to the unitary digital-to-analog converter,

wherein the digital signal processor comprises a multiport quantizer converting a plurality of multi-bit multiport inputs to a single-bit multiport output, and

wherein the digital signal processor comprises at least one higher-order shaper circuit to spectrally shape nonlinear intersymbol interference (NLISI).

6. The converter of claim 5, wherein the multiport quantizer comprises:

a plurality of weights (w_1, w_2 ... w_k), to be multiplied by each input of the plurality of multi-bit multiport inputs, thus forming a plurality of weighted products;

a multiport summer, to sum the plurality of the weighted products; and

a quantizer, to provide the single-bit multiport output, the sign of the single-bit multiport output depending on the sign of the plurality of the weighted products.

7. The converter of claim 5, wherein the multiport quantizer comprises:

a first plurality of summers, wherein each input of the plurality of multi-bit multiport inputs is summed to a positive value, thus obtaining a first plurality of tentative quantization errors;

a second plurality of summers, wherein each input of the plurality of multi-bit multiport inputs is summed to a negative value, thus obtaining a second plurality of tentative quantization errors;

a first plurality of squaring circuits, each squaring circuit of the first plurality squaring a respective tentative quantization error of the first plurality of tentative quantization errors, thus obtaining a first plurality of squared tentative quantization errors;

a second plurality of squaring circuits, each squaring circuit of the second

plurality squaring a respective tentative quantization error of the second plurality of tentative quantization errors, thus obtaining a second plurality of squared tentative quantization errors;

a first multiport summer, to sum the first plurality of squared tentative quantization errors;

a second multiport summer, to sum the second plurality of squared tentative quantization errors; and

a comparator, to compare the first plurality of squared tentative quantization errors with the second plurality of tentative quantization errors and to provide the single-bit multiport output.

8. The converter of claim 7, wherein the sign of the single-bit multiport output is positive if the first plurality of squared tentative quantization errors is greater than the second plurality of squared tentative quantization errors and is negative if the second plurality of squared tentative quantization errors is greater than the first plurality of squared tentative quantization errors.

9. The converter of claim 5, wherein said at least one higher-order shaper circuit comprises:

a delay element to remember a previous value of the single-bit multiport output;

a first multiplier element connected to the delay element and calculating a product proportional to an order of nonlinear intersymbol interference corresponding to the order of the higher-order shaper circuit;

a digital filtering element to spectrally shape the product calculated by the first multiplier element; and

a second multiplier element connected to the digital filtering element and generating a bias signal, said bias signal forming a multi-bit multiport input of the plurality of the multi-bit multiport inputs.

10. The converter of claim 5, wherein higher i-order NLISI is spectrally shaped with a transfer function $W_i(z) = 1 / (1 - H_i(z))$ and wherein $H_i(z)$ indicates a transfer function of a higher i-order digital filtering element.

11. An oversampling digital-to-analog converter comprising:

a first digital filter having a first digital filter input and a first digital filter output, said first digital filter being for filtering an input signal having a signal band;

a second digital filter having a second digital filter input and a second digital filter output, said second digital filter being for filtering a quantized signal;

a summing element having a summing element output, said summing element for summing said first digital filter output with said second digital filter output wherein said second digital filter and said summing element form a first order shaper circuit, said summing element being a first order bias signal;

at least one higher-order shaper circuit, said at least one higher-order shaper circuit generating a higher-order bias signal, said higher-order bias signal indicating magnitude of a portion of nonlinear intersymbol interference (NLISI) falling in the signal band;

a multiport quantizer having a plurality of multiport quantizer inputs and a multiport quantizer output, said plurality of multiport quantizer inputs comprising said first order bias signal and said higher-order bias signal;

a feedback loop for connecting said multiport quantizer output to said first digital filter input and to said at least one higher-order shaper circuit;

a unit element digital-to-analog converter having a unit element digital-to-analog converter output, said unit element digital-to-analog converter being connected with said multiport quantizer output; and

a continuous time filter connected to said digital-to-analog converter output.

12. The converter of claim 11, wherein said higher-order bias signal indicates magnitude of a second order product of said NLISI.

13. The converter of claim 11, further comprising a second higher-order shaper circuit for generating a second higher-order bias signal indicating magnitude of a third order product of said NLISI.

14. The converter of claim 12 wherein said at least one shaper circuit for generating said bias signal indicating said magnitude of said second order product of said NLISI comprises:

a first delay element, having a first delay element input and a first delay element output, said first delay element input being connected with said multiport quantizer output via said feedback loop;

a first multiplier element having a first multiplier output, said first multiplier element for multiplying said first delay element output with said multiport quantizer output;

a third digital filter, having a third digital filter input and a third digital filter output, said third digital filter being connected with said first multiplier element output, said third digital filter for isolating said second order product of said NLISI; and

a second multiplier element having a second multiplier element output, said second multiplier element for multiplying said third digital filter output with said multiport quantizer output, said second multiplier element output being connected with one input of said multiport quantizer, said second multiplier output providing said higher-order bias signal indicating said magnitude of said second order product of said NLISI.

15. The converter of claim 14, further comprising a second higher-order shaper circuit for generating a second higher-order bias signal indicating magnitude of a third order product of said NLISI.

16. The converter of claim 15, wherein said second higher-order shaper circuit comprises:

a second delay element having a second delay element input and a second delay element output, said second delay element input being connected with said first delay element output;

a third multiplier element having a third multiplier element output, said third multiplier element for multiplying said second delay element output with said first multiplier element output;

a fourth digital filter having a fourth digital filter input and a fourth digital filter output, said fourth digital filter input being connected with said third multiplier element output for isolating said third order product of said NLISI; and

a fourth multiplier element having a fourth multiplier element output, said fourth multiplier element for multiplying said fourth digital filter output with said first

multiplier element output.

17. The converter of claim 16, wherein said fourth multiplier element output is connected to one input of said multiport quantizer for providing a bias signal indicating said magnitude of said third order product of said NLISI.

18. The converter of claim 14, wherein the third digital filter has a transfer function $H_2(z) = 1/(z-1)$.

19. The converter of claim 11, further comprising additional higher-order shaper circuits for generating additional higher-order bias signals indicating magnitude of higher-order products of said NLISI.

20. The converter of claim 19, wherein each of the additional higher-order shaper circuits comprises a higher-order digital filter.